

New NASA satellite-to-satellite communications take shape



By *Peter Simmons*

In this article Peter summarizes the evolution of today's Tracking and Data Relay Satellite System (TDRSS) and describes how a software reconfigurable platform with heterogeneous transceiver architecture addresses the need to simulate satellite-to-satellite links.

The National Aeronautics and Space Administration (NASA) Goddard Space Flight Center's Cross Link Integrated Development Environment (CLIDE) program is currently developing technologies to facilitate new satellite-to-satellite communications, enabling lower cost constellations of satellites to provide critical scientific data in a timely fashion. These direct satellite-to-satellite links allow for mesh connectivity and ad hoc networking, thereby ensuring that a satellite communications network can reliably provide full coverage of the earth, a key requirement for future NASA missions.

Starting in the late 1950s NASA's method for providing data communications from orbiting satellites consisted of a network of powerful antennas at ground stations located around the world. The major disadvantage to this system was that the time available to communicate with the orbiting satellites as they passed overhead was very limited. As the number of satellites placed into orbit increased, researchers determined that a series of geostationary satellites could provide nearly continuous tracking and data transfer capabilities. The idea for a global system of communication satellites was developed through the 1970s and culminated with the launch of the first tracking and data relay satellite, TDRS-1, in 1983. Following the loss of TDRS-2 in the Challenger accident in 1986, five more TDRS satellites were launched over the next nine years to create the global coverage NASA provides

today. In 2000 TDRS-H (now known as TDRS-8), the first of the Replenishment Spacecraft, was launched¹.

The TDRSS, consists of seven tracking and data relay satellites (six original satellites built by TRW and one replenishment satellite built by Boeing Satellite Systems), two ground terminals at the White Sands Complex in New Mexico, a ground terminal extension on the island of Guam, and customer and data handling facilities. This constellation of satellites provides global communication and data relay services for the Space Shuttle, International Space Station (in the future), Hubble Space Telescope, and a multitude of low earth orbiting satellites, balloons, and research aircraft.² The existing seven craft are nearing their end of life and are being replaced by TDRS H, I, and J satellites, which completed on-orbit testing in 2003.

The functional and technical performance requirements for TDRS H, I, and J satellites are virtually identical to those of the current satellites except for improved multiple access and S-band single-access performance, addition of Ka-band, and spacecraft collocation³. These new higher-frequency (22.5 GHz to 27.5 GHz) services increase data rate capabilities to 800 Mbps in order to support future missions requiring higher bandwidth communications such as multi-spectral instruments for Earth science applications.⁴

The CLIDE development environment required hardware that could be used to modulate and demodulate a 6 MHz bandwidth Quadrature Phase Shift Keying (QPSK) data channel in order to simulate satellite-to-satellite links (such as those used by the TDRSS satellites). As this is a development project, NASA was looking for a vendor that could offer waveform development expertise as well as provide ongoing hardware and software support.

NASA requirement #1: flexible, reconfigurable transceiver architecture for rapid prototyping

NASA's application required a reconfigurable transceiver capable of handling a 3 megabaud QPSK waveform with decision directed feedback for carrier loop recovery. The waveform needed to demodulate a test data stream with no bit errors. The hardware had to accommodate other waveforms such as CDMA and FDMA, having different data rates, modulation schemes, and channel coding.

NASA used three identical systems to simulate three satellites. Initially, only the receive processing path, shown in Figure 1, was tested.

The receive processing path had the following requirements:

- Direct sampled down conversion of one channel at 70 MHz IF.
- Support one 6 MHz bandwidth data channel.
- Provide up to 300 KBps sustained data rates for the received channel.
- Sustain 600 KBps continuous data transfer from the receiver DSP to the system host processor.

Future tests will include a transmit processing path, which will have the following requirements:

- Ability to sustain up to 300 KBps continuous data transfer from system host processor to TX DSP.
- Modulation to spread the spectrum to 6 MHz.
- Direct up conversion to an IF of 70 MHz.

Other system requirements for the initial tests included:

- Hardware and driver level software accessible to NASA developers.
- CompactPCI backplane.
- COTS hardware and software tools.
- Low cost of iteration.

The rapid prototyping of different waveforms required the ability to assemble different hardware components quickly and easily in order to reduce the time scheduled for testing.

Spectrum's SDR-3000 solution

Hardware

NASA chose Spectrum's *flexComm* product line, specifically the SDR-3000 software reconfigurable platform, for its heterogeneous processing transceiver architecture. This two-slot CompactPCI based hot swappable architecture provides the following processing boards:

- An analog I/O board (TM1-3300) supporting four 14-bit, 80 MSps Analog Devices AD6645AST-80 ADCs and four 14-bit, 160 MSps Analog Devices AD9772AAST DACs.
- A front end processing board (PRO-3100) supporting four user programmable Xilinx Virtex-II XC2V6000 FPGAs, each having 6 million gates.
- A signal processing board (PRO-3500) supporting up to four 450 MHz G4 PowerPC MPC 7410 processors with the AltiVec engine and/or additional I/O via two ePMC mezzanine sites.

Figure 2 shows the data flow diagram of an SDR-3000 system. The receive processing path, implemented for the cross-link simulator is described here.

The 70 MHz return link was supplied to the input of the TM1-3300 analog I/O board. One AD6645AST-80 ADC can digitize up to a 40 MHz bandwidth centered at 70 MHz. Therefore, only one of the four AD6645AST-80s was used to digitize the 6 MHz channel of interest. See Figure 2 (A).

The 160 MBps digital signals are packed and sent out over the TM1-to-PRO-3100 interface to the Virtex-II XC2V6000 FPGAs on the PRO 3100 (B). The first Virtex-II XC2V6000 FPGA (C) has the following logic implemented:

- A wideband DDC core to produce the I and Q outputs at a lower data rate of 64 Mbps.
- A 3 megabaud fixed frequency Synchronization Circuit.

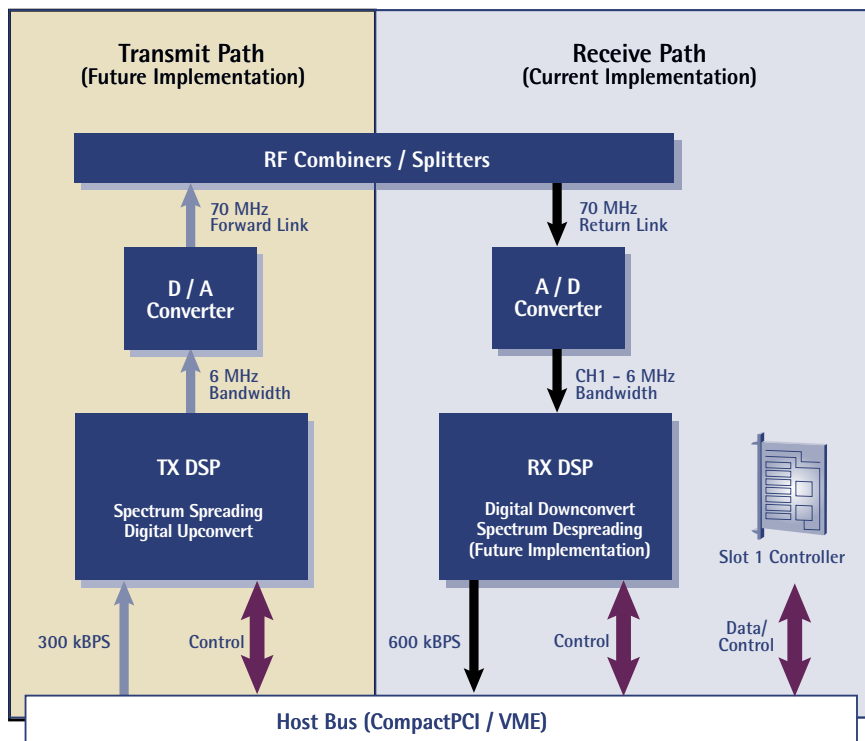


Figure 1

- A QPSK Symbol Decode/Phase Compute/Carrier Recovery Feedback Loop. A Xilinx LogiCore Cordic core will compute phase of the I and Q data from the wideband DDC. This phase will be converted to phase error using the symbol decode outputs, and the phase error will be fed back into the wideband DDC through a loop filter, completing the carrier recovery loop.

The output of the Symbol Decoder circuit of the Virtex-II XC2V6000 FPGA goes to the Front Panel I/O (not shown) on the PRO-3100 board and then to a host processor via Ethernet (implemented by NASA).

The transmit data path, required for future implementations, is essentially the opposite of the receive data path. Data flows on separate unidirectional links, except for the data on the CompactPCI bus.

In this example, one Virtex-II XC2V6000 FPGA implements the DDC and the symbol decoder. The SDR-3000 can partition the waveform across multiple, heterogeneous processors by using a switched fabric such as Spectrum's Rapid I/O based *flexFabric* (D) and the backplane (E). The *flexFabric* supports up to 320 MBps, which is more than the 300 Kbps required for this application.

For a waveform in which the Virtex-II XC2V6000 FPGAs are dedicated to chan-

nelization and/or down conversion, the symbol decoding can be implemented using the PowerPC G4 7410s (F) or TI C64X DSPs on mezzanine boards. This modular architecture supports many different combinations of signal processing engines in two slots of a CompactPCI chassis.

In addition to easily changing the hardware configuration of the SDR-3000, the Virtex-II XC2V6000 FPGAs can be reconfigured to support different waveforms. Therefore, the data flow from IF to baseband can be optimized quickly and easily for each waveform that NASA plans to test.

Software and application development

The bandwidth and complexity of the QPSK waveform is too great for a complete software implementation and therefore required the processing power of the Virtex-II XC2V6000 FPGA. The QPSK waveform was implemented on 25 percent (or 1.5 million gates) of a single Virtex-II XC2V6000 FPGA processor of the SDR-3000. The SDR-3000 could therefore implement 16 of these QPSK waveforms or a combination of these and other waveforms.

The decision directed QPSK waveform can be extended to one of the standard 16 QAM PSK modulation schemes. Other modulation schemes, including narrowband QPSK waveforms, can also be easily accommodated by this design.

The transceiver design of the SDR-3000 allows NASA to implement modulation waveforms in addition to the demodulation waveforms that were demonstrated.

Spectrum's complete software operating environment includes real-time operating systems (Wind River's VxWorks, Texas Instruments' DSP/BIOS), a hardware abstraction layer (*quicComm*), standards based communication protocols, (POSIX Messaging, TCP/IP, TAO, CORBA), and an application abstraction layer supporting component based application development and deployment (Software Communications Architecture core framework). This layered software stack provides access to hardware level drivers for optimum hardware performance or can abstract the hardware to allow for greater code portability.

Spectrum delivered a working waveform with the hardware platform, which saved NASA two months of development time and kept their demonstration project on schedule.

NASA requirement #2: strong technical support and customer understanding

The highly technical nature of the problem being solved and the complex technical environment led NASA to look for a supplier that could deliver a high quality product, train NASA engineers on using the product, and provide ongoing support during the development of the cross-link simulator.

The on-site support Spectrum provided NASA ranged from delivering training courses on the SDR-3000 to field upgrading the firmware and consulting on the development of their waveform.

"Spectrum's *flexComm* signal processing technology met our requirements and the system was delivered on cost and on schedule."

— Jason Soloff, Program Manager, NASA CLIDE program

Spectrum's technical support team delivered a three-day training workshop on the SDR-3000 to NASA's engineers. This provided the engineers with a fast, cost-effective way of acquiring the knowledge necessary to develop real-time applications on Spectrum's SDR-3000 platforms.

The field application engineers accelerated NASA's development effort by providing a source code demodulation implementation example and giving training on the implementation. Spectrum's engineers worked with NASA on an ongoing basis to develop their application and dataflow. NASA was able to develop its application quickly and efficiently knowing that the Spectrum technical team was available for on-site consultation at short notice.

Conclusion

The SDR-3000 demonstrated the ability to demodulate a 6 MHz wide 3 megabaud QPSK signal. One channel was digitized using one of the four AD6645AST-80 ADC and the signal demodulated using 25 percent of one Virtex-II XC2V6000 FPGA processor. Therefore, a single SDR-3000 system could process up to 16 similar receive channels, exceeding the technical requirements for one of the systems of the cross-link simulator. Future tests using the transmit path can be accom-

modated with the Virtex-II XC2V6000 FPGA processors implementing up converter and spread spectrum circuits. Waveforms could also be partitioned, with the PowerPC G4 7410s and/or the TI C64X handling the baseband processing while the Virtex-II XC2V6000 FPGAs do the up/down conversions and channelization. For example, one implementation could allow the SDR-3000 to process eight receiver channels and eight transmit channels.

Spectrum's on-site training workshop gave the NASA developers a solid foundation in using the SDR-3000. Spectrum then worked together with NASA to develop the QPSK demodulator. This combined development effort ensured that NASA completed its demonstration project on time and on budget.

"Spectrum's *flexComm* signal processing technology met our requirements and the system was delivered on cost and on schedule," said NASA's Jason Soloff, program manager for the NASA CLIDE program.

1, 2, 3 <http://tdrs.gsfc.nasa.gov/tdrsproject/about.htm#history>, accessed 12/16/2003

4 http://www.gsfc.nasa.gov/gsfc/service/gallery/fact_sheets/spacesci/tdrs_hij.htm, accessed 12/16/2003

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Pictured: Mobile CompactPCI chassis, industrial PC, PRO-3100 FPGA and PRO-3500 Power PC processing engines, TM1-3300 transition module, Tornado IDE and VxWorks screen shots.